6. (Amended) The apparatus of claim 5, wherein the system management interrupt handler instructions stored in the system main memory are part of a basic input/output system (BIOS).

8. (Amended) A method, comprising:

receiving a system management interrupt acknowledge signal from a processor; and

fetching a plurality of system management interrupt handler instructions from an integrated system management memory in a memory controller regardless of a system management memory address indicated by the processor in response to the system management interrupt acknowledge signal.

9. Cancelled

10. (Amended) The method of claim 8, further comprising latching the system management memory address indicated by the processor.

19. (Amended) The system of claim 18, wherein the system management interrupt handler instructions stored in the system main memory are part of a basic input/output system (BIOS).

REMARKS

In the Office Action dated September 13, 2001, claims 1-20 are noted as pending. Claims 1-5, 7, 14-18, and 20 are noted as allowed. Claims 6, 9-13, and 19 are noted as being objected to. Claim 8 is rejected under 35 USC 102(e) as being anticipated by Shiell et al., U.S. Patent No. 5,954,812 (Shiell). Claim 9 is cancelled.

CONCLUSION:

In view of the foregoing, Applicant submits that claims 1-8, and 10-20 are distinguished over the cited art and are in condition for allowance. Allowance of claims 1-8 and 10-20 is respectfully requested.

DEPOSIT ACCOUNT AUTHORIZATION

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Dated: 12/27/01

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Date

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the claims:

6. (Amended) The apparatus of claim 5, wherein the system management interrupt handler instructions stored in the system main memory are part of a [basis] basic input/output system (BIOS).

8. (Amended) A method, comprising:

receiving a system management interrupt acknowledge signal from a processor; and

fetching a plurality of system management interrupt handler instructions from an integrated system management memory in a memory controller regardless of a system management memory address indicated by the processor in response to the system management interrupt acknowledge signal.

9. Cancelled

10. (Amended) The method of claim [9] 8, further comprising latching the system management memory address indicated by the processor.

19. The system of claim 18, wherein the system management interrupt handler instructions stored in the system main memory are part of a [basis] basic input/output system (BIOS).

Claims 6 and 19 have been amended in order to cure the informalities noted by the Examiner.

REJECTIONS UNDER 35 U.S.C. 102(e)

Claim 8 is rejected under 35 USC 102(e) as being anticipated by Shiell. However, Shiell does not disclose

> fetching a plurality of system management interrupt handler instructions from an integrated system management memory in a memory controller regardless of a system management memory address indicated by the processor in response to the system management interrupt acknowledge signal
> (Amended claim 8, emphasis added).

Therefore, claim 8 is not anticipated by the Shiell reference. Claims 10-13, which depend from claim 8, are likewise not anticipated by the Shiell reference.